

B: Amendments to The Claims:

1 1. (currently Amended) A method for providing an area
2 optimized binary orthogonality checker ~~for a scalable~~
3 ~~selector system for controlling data transfers and routing~~
4 ~~in a data processing system~~ comprising the steps of:

5 determining ~~the~~ a logical gate count for an implementation
6 of an orthogonality checker for a scalable selector system
7 for controlling data transfers and routing in a data
8 processing system, and minimizing the gate count and an
9 area needed to implement an orthogonality checker given a
10 library of logical gates to implement the circuit and ~~the~~
11 given an area for each gate in the library and to optimize
12 an hierarchical orthogonality structure for said
13 hierarchical design of said circuit while maintaining a
14 hierarchical design for a circuit.

1 2. (Original) The method according to claim 1 including the
2 steps of: determining the optimal mix of hierarchical
3 level, and determining ~~the~~ inputs to implement a given
4 orthogonality checker to achieve the minimized circuit.

1 3. (Original) The method according to claim 1, where the
2 area of a binary orthogonality checker is implemented in a
3 static CMOS circuits by minimizing the logical gate count
4 and an area needed for checker implementation given a
5 library of logical gates to implement the circuit and the
6 area ~~for~~ of each gate in the library.



1 4. (Original) The method according to claim 3, including a
2 step of determining an optimal mix of hierarchical levels
3 and inputers to implement a given orthogonality checker to
4 achieve the minimized circuit.

1 5. (Original) The method according to claim 4 wherein said
2 orthogonality checker is employed in a scalable selector
3 system for controlling data transfers and routing in a data
4 processing system, comprising a plurality of input data
5 buses coupled to a multiple-bit, multiple bus selector
6 having data, data valid, and an orthogonality check outputs
7 and having multiple data input bus ports coupled for
8 receipt of signal from said plurality of input data buses.

1 6. (Currently Amended) The method according to claim 5
2 wherein after determining an expected number for the
3 logical gate count ~~for~~ of an implementation of an
4 orthogonality checker, and the binary orthogonality
5 checking is provided by hierarchically combining the checks
6 with smaller numbers of inputs and by performing ~~the~~ a
7 total check of a large number of inputs with less gates and
8 in a smaller area.

1 7. (Original) The method according to claim 1 wherein
2 after determining an expected number for the gate count,
3 multiple checks are combined with reduced input sets ~~are~~
4 ~~combined~~ into one larger check and the orthogonality
5 checking is performed, with a check on each input set, as
6 well as combining an OR of all the inputs to the check.



1 8. (Original) The method according to claim 7 wherein the
2 resulting OR values are then checked for orthogonality, and
3 the results of all the checks are Ored together.

1 9. (Original) The method according to claim 8 wherein the
2 structure for orthogonality check is extended to multiple
3 hierarchical levels and works with orthogonality checks
4 said extended size implementation.

1 10. (Original) The method according to claim 9 wherein the
2 structure determined is an optimal hierarchical structure
3 for a given library and a given number of inputs to check.-